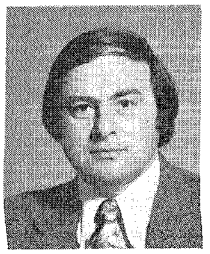
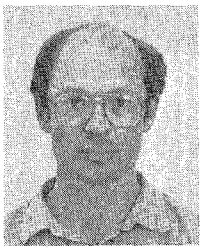
converter," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 716–719, Oct. 1978.
[3] P. J. Meier, "Integrated fin line millimeter components," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 1209–1216, Dec. 1974.
[4] W. J. R. Hoefer, "Fin line design made easy," presented at the *1978 IEEE-MTT-S Int. Microwave Symp.* (Ottawa, Canada).
[5] S. B. Cohn, "Properties of ridge waveguide," *Proc. IRE*, vol. 35, pp. 783–788, Aug. 1947.
[6] S. Hopfer, "The design of ridged waveguides," *IRE Trans. Microwave Theory Tech.*, vol. MTT-3, pp. 20–29, Oct. 1955.
[7] T.-S. Chen, "Calculation of the parameters of ridge waveguide," *IRE Trans. Microwave Theory Tech.*, vol. MTT-5, pp. 12–17, Jan. 1957.
[8] N. Marcuvitz, *Waveguide Handbook*, MIT Radiation Lab. Series, no. 10, Boston Technical Publishers Inc., 1964.
[9] W. J. Getsinger, "Ridge waveguide field description and application to directional couplers," *IRE Trans. Microwave Theory Tech.*, vol. MTT-10, pp. 41–50, Jan. 1962.
[10] A. K. Sharma, G. Costache, and W. J. R. Hoefer, "Cutoff in fin lines evaluated with the spectral domain technique and with the finite element method," in *1981 IEEE/AP Int. Symp. Dig.*, (Los Angeles, CA), pp. 308–311.
[11] H. A. Wheeler, "Coupling holes between resonant cavities or waveguides evaluated in terms of volume ratios," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-12, pp. 231–244, Mar. 1964.
[12] H. Hofmann, private communication.
[13] H. Meinel and B. Rembold, "New millimeter-wave fin line attenuators and switches," in *1979 IEEE-MTT-S Int. Microwave Symp. Dig.*, (Orlando, FL), pp. 249–251.
[14] A. K. Sharma and W. J. R. Hoefer, "Empirical expressions for fin line design," accepted for publication in the *IEEE Trans. Microwave Theory Tech.*, Apr. 1983.
[15] Y. C. Shih and W. J. R. Hoefer, "The accuracy of TLM-analysis of finned rectangular waveguides," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 743–746, July 1980.



Wolfgang J. R. Hoefer (M'71–SM'78) was born in Urmitz/Rhein, Germany, on February 6, 1941. He received the diploma in electrical engineering from the Technische Hochschule Aachen, Aachen, Germany, in 1964, and the D.Ing. degree from the University of Grenoble, Grenoble, France, in 1968.

After one year of teaching and research at the Institut Universitaire de Technologie, Grenoble, France, he joined the Department of Electrical Engineering, the University of Ottawa, Ottawa, Ont., Canada, and is currently a Professor in this department. During a sabbatical year in 1976–77, he spent six months with the Space Division of the AEG-Telefunken in Backnang, Germany, and six months with the Institut National Polytechnique de Grenoble, France. His research interests include microwave measurement techniques, millimeter-wave circuit design, and numerical techniques for solving electromagnetic problems.

Dr. Hoefer is a registered Professional Engineer in the Province of Ontario, Canada.



Miles N. Burton was born in Neepawa, Manitoba, in 1950. He received the B.Sc.E.E. degree from the University of Manitoba in 1980.

From 1980 to 1981 he worked in the Security Systems Division of Computing Devices Co. in Ottawa, Canada. Since 1981 he has been a graduate student in the Department of Electrical Engineering, University of Ottawa. His research activities are in the area of microwave circuits.

A Compact Broad-Band Multifunction ECM MIC Module

EDWARD C. NIEHENKE, SENIOR MEMBER, IEEE, RICK D. HESS, MEMBER, IEEE, JED S. ROSEN, LAWRENCE E. DICKENS, FELLOW, IEEE, AND JOSEPH A. FAULKNER, JR., MEMBER, IEEE

Abstract—**A development effort is described that yielded a compact broad-band ECM module using soft and hard substrate material employing microstrip, slotline, and coplanar line. Integrated functions include coupling, limiting, upconversion, downconversion, broad-band amplification, amplitude modulation, switching, gating, and stable frequency generation. A high-level frequency converter with a +28-dBm intercept point resulted in high dynamic range, spurious-free operation (−45 dBc). Extremely flat amplification with low-current drain is achieved with distributed and cascode FET amplifiers at *S*–*C* and *X*-bands.**

Manuscript received April 19, 1982; revised July 22, 1982.

E. Niehenke, J. Rosen, L. Dickens, and J. Faulkner are with Westinghouse Electric Corp., Baltimore, MD 21203.

R. Hess was with Westinghouse Electric Corp., Baltimore, MD, and is now with Stable Energy Sources, Lancaster, PA 17603.

I. INTRODUCTION

REDUCING THE size, weight, and power consumption of modern electronic systems requires compact, efficient, plug-in, multifunction modules. Key parameters are broad bandwidth, flat frequency response, low power consumption, high speed, high dynamic range, and low spurious signal generation. This paper describes details of the microwave substrate materials and layout to miniaturize

0018-9480/82/1200-2194$00.75 ©1982 IEEE

the module. This module includes nine basic functions and 19 individual circuits. The design and experimental performance of the various circuit functions are presented with emphasis on the high-level, high dynamic range, frequency converter; ultrastable, high-power dielectric resonator FET oscillator; and two FET amplifiers: the distributed and the cascode amplifiers.

II. Description

A. Module Function

The module function is to convert an *X*-band RF signal to an IF signal (2.6 to 5.2 GHz) with its own internal *Ku*-band dielectric resonator FET oscillator (DRO). At IF, the signal is amplified, split, and switched between various IF channel paths that are gated, amplified, and attenuated with a linear voltage variable attenuator (VVA). The IF signal is outputted three places and inputted two places. Finally the signal is upconverted to *X*-band and, using the same DRO signal, amplified and outputted.

B. Module Layout

Fig. 1 illustrates the compact 7.1-in × 4.2-in × 0.8-in MIC 20-oz module. This module is plugged into external circuitry through the use of low VSWR spring-loaded RF connectors developed by Selectro Corporation. This module contains one *X*-band limiter, three 60-dB multipole IF switches, two frequency converters, five couplers, four IF amplifiers with a total gain of 80 dB, two 25-dB VVA's, one 36-dB *X*-band RF limiting amplifier, and one DRO.

To prevent RF coupling between the circuit functions, to minimize ground plane discontinuities, and to provide lower level testability, the components were distributed among nine individual assemblies placed within a one-piece channelized case. Eight of the nine substrates are visible in Fig. 1; the DRO and a one-piece printed circuit board containing the control and bias circuitry are on the opposite side. The soft substrate assemblies are made of either 0.015-in-thick Rogers 5880 Duroid ($\epsilon_r = 2.2$) or 0.025-in-thick 3-M Epsilam 10 ($\epsilon_r = 10.2$) dielectric laminated to a 0.10-in-thick aluminum plate. Drop-in alumina substrates (0.025 in thick) containing 3-dB RF and IF Lange couplers or switch circuitry are bonded into pockets in the soft substrate assemblies. The FET's and p-i-n diodes are soldered to small gold-plated copper pedestals attached to the ground plane. Covers on both sides are soldered to the plated aluminum chassis, sealing the entire unit hermetically.

C. Distributed Amplifier

A newly developed distributed amplifier simultaneously achieves constant gain and low VSWR over an octave frequency range. It has low power consumption in a small size. The circuit exhibits high reverse isolation and unconditional stability, and it may be readily cascaded to achieve higher gains.

Low VSWR and constant gain over an octave bandwidth with unconditional stability is achieved using matched lumped-element input and output transmission lines with a

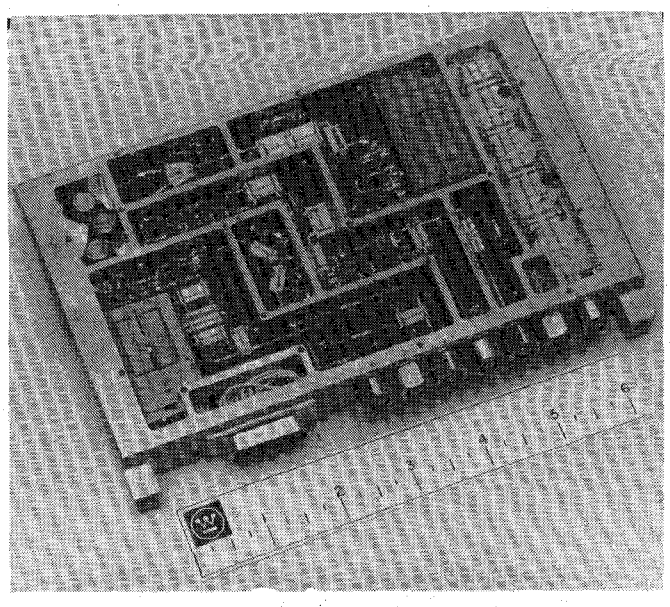


Fig. 1. MIC module.

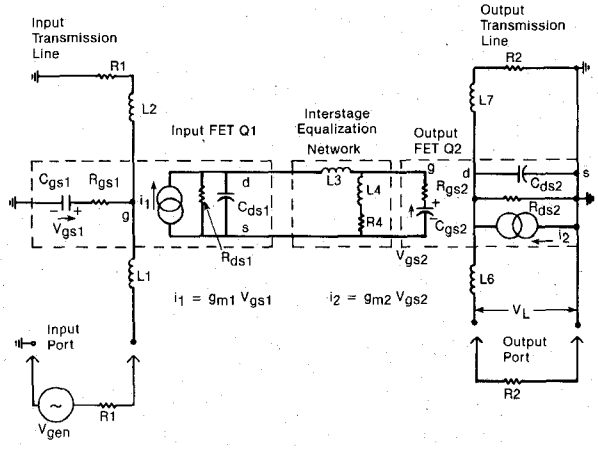


Fig. 2. Distributed amplifier equivalent circuit.

FET embedded in each line. They are coupled with an interstage gain equalization network as depicted in Fig. 2. The input distributed line consists of the series inductor $L1$, the input FET $Q1$ series resistance–capacitance ($R_{gs1}-C_{gs1}$) elements to ground, and the series inductor $L2$ terminated with resistance $R1$ (50 Ω). The output distributed line consists of the series inductor $L7$, the parallel resistance–capacitance ($R_{ds2}-C_{ds2}$) of the output FET $Q2$ to ground, and the series inductor $L6$ to ground terminated with $R2$ (50 Ω). Good input and output match is obtained by equating the characteristic impedance of the lumped-element transmission lines to the source and load resistances, both assumed to be equal to 50 Ω. This relationship is expressed below with the accompanying range of angular frequencies (ω) for which good match (less than 1.3 : 1 VSWR) exists with $L1 = L2$ and $L6 = L7$

$$R1 = \sqrt{\frac{2L1}{C_{gs1}}}, \qquad 0 \leqslant \omega \leqslant \frac{1}{C_{gs1}R1}$$

$$R2 = \sqrt{\frac{2L6}{C_{ds2}}}, \qquad 0 \leqslant \omega \leqslant \frac{1}{C_{ds2}R2}.$$

TABLE I
POLAR S-PARAMETERS FOR DEXCEL 2501 CHIP

Frequency (MHz)	S11 Magn	S11 Angl	S21 Magn	S21 Angl	S12 Magn	S12 Angl	S22 Magn	S22 Angl	S21 (dB)	K Factor	Gmax or MSG (dB)
2500	0 92	43	2 44	140 4	0 039	69 4	0 71	-14	7 75	0 48	18 0
3000	0 89	-52	2.36	133 0	0 044	66 0	0 70	-17	7 46	0 58	17 3
3500	0 86	-60	2 27	125 7	0 048	62 9	0 68	-20	7 12	0 71	16 7
4000	0 83	-67	2 16	119 0	0 050	61 0	0 66	-23	6 69	0 87	16 4
4500	0 81	-74	2 04	113 4	0 052	60 9	0 65	-26	6 19	0 95	15 9
5000	0 79	-80	1 93	108 4	0 053	62 0	0 64	-29	5 71	1 05	14 2
5500	0 77	-86	1 84	103 9	0 054	63 5	0 63	-32	5 30	1 16	12 9

The interstage equalization network ($L3$, $L4$, $R4$) simultaneously matches $Q1$ to $Q2$ at the high-frequency end of the band with minimal loss of gain due to $R4$ and equalizes the gain over frequency through mismatch as well as resistive loss in $R4$ at lower frequencies.

Dexcel 2501 FET chips used for both stages were operated at 3.5 V and 20 mA. They have a 1-μm gate length and 500-μm gate width. The S-parameters including wire bond leads are listed in Table I. In evaluating $S11$ and $S22$, $R_{gs} = 15\ \Omega$, $R_{ds} = 250\ \Omega$, $C_{gs} = 0.5$ pF, and $C_{ds} = 0.2$ pF.

The circuit is analyzed with an equivalent circuit as shown in Fig. 2 in terms of three voltage coupling factors, namely $K1$, $K2$, and $K3$. Their product $(K1 \cdot K2 \cdot K3)$ relates the voltage developed across the load (V_L) to the voltage available across the amplifier's input port ($0.5\ V_{\text{gen}}$) for maximum power transfer. The power gain of the amplifier for equal source and load resistance values ($R1 = R2$) is $(K1 \cdot K2 \cdot K3)^2$. The input voltage coupling factor is the ratio of the voltage developed across the gate-to-source capacitance of the input FET (V_{gs1}) to the voltage $0.5\ V_{\text{gen}}$. The interstage voltage coupling factor ($K2$) is the ratio of the voltage across the gate-to-source capacitance of the second FET (V_{gs2}) to V_{gs1}. Finally, the output coupling factor ($K3$) is the ratio of the voltage developed across the load (V_L) to V_{gs2}.

Equation (1) expresses $K1$ as a function of the input circuit parameters

$$K1 = \frac{V_{gs1}}{0.5\ V_{\text{gen}}} = \frac{1}{\left(1 - \dfrac{\omega^2 L1 C_{gs1}}{2}\right) + j\omega C_{gs1}\left(R_{gs1} + \dfrac{R1}{2}\right)}. \tag{1}$$

At low frequencies, K_1 is exactly equal to 1 (0-dB power loss). At higher frequencies, the real part of the denominator decreases from unity while the imaginary part increases from zero; the result is a nearly constant $K1$ when the transmission line is matched, i.e.,

$$R1 = \sqrt{\frac{2L1}{C_{gs1}}} \quad \text{and} \quad \omega \leqslant \frac{1}{C_{gs1} R1}.$$

The frequency range for which the input circuit is matched and $K1$ is constant is relatively wide.

The voltage coupling of the output circuit transfer function ($K3$) from the input voltage across the output FET (V_{gs2}) to the load (V_L) is also relatively independent of frequency because C_{ds2} is embedded in a matched output transmission line. This coupling is expressed as

$$K3 = \frac{V_{\text{out}}}{V_{gs2}} = \frac{0.5 g_{m2} R_2}{\left(1 + \dfrac{R2}{2R_{ds2}} - \dfrac{\omega^2 L6 C_{ds2}}{2}\right) + j\left(\dfrac{\omega C_{ds2} R_2}{2} + \dfrac{\omega L6}{2R_{ds2}}\right)} \tag{2}$$

where $L6 = L7 =$ output line inductance, and $g_{m2} =$ transconductance of output FET.

Again, $K3$ for a matched output transmission line condition is relatively independent of frequency and is equal to $0.5 g_{m2} R2/(1 + R2/2R_{ds2})$. For the FET used, $g_m = 0.033$ mho, resulting in a $(K1 \cdot K3)^2$ of -2.5 dB, which compares closely with computer-generated loss values of -2.7 to -2.3 dB, respectively, across the 2.5 to 5.5-GHz band, with a maximum input and output VSWR of 1.3 : 1 considering both input and output circuits. The use of two FET's significantly improves the amount of gain that can be achieved per section of a distributed amplifier of this type. The use of one FET per section [1] requires many stages to obtain comparable gain.

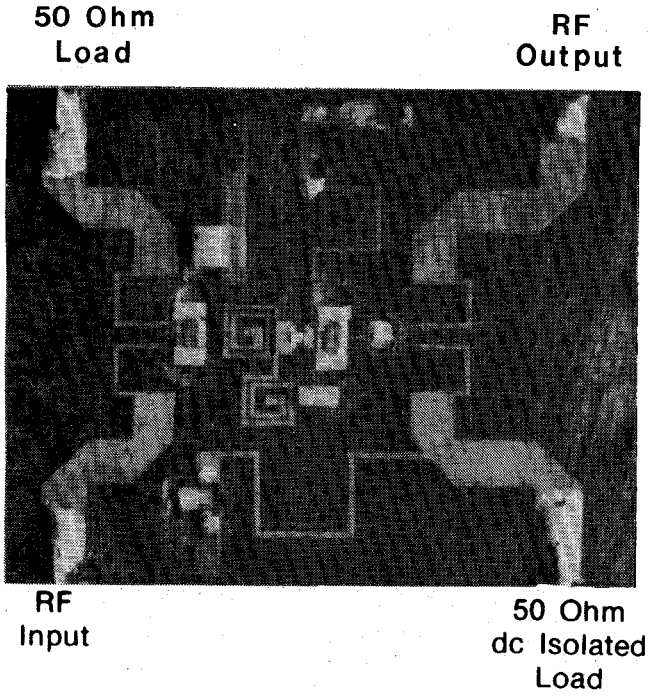
The input and output circuits make the potentially unstable FET unconditionally stable for any input or output load regardless of the interstage equalization network. This feature was determined by examining the stability factor and stability locations of input and output circuits individually.

The interstage coupling factor between the input voltage across C_{gs1} of $Q1$ to the input voltage across C_{gs2} of $Q2$ depends on the interstage equalization network as well as the transconductance of the first FET (g_{m1}). Intuitively, maximum transfer occurs when the output impedance of the first FET is transformed to the complex conjugate of the input impedance of the second FET, which is indeed the situation when the analysis is performed (neglecting feedback) as expressed in (3)

$$K2(\max) = \left(\frac{V_{gs2}}{V_{gs1}}\right)_{\max} = \frac{g_{m1}}{2\omega C_{gs2}} \sqrt{\frac{R_{ds1}}{R_{gs2}}} \tag{3}$$

where $R_{ds1} =$ drain-to-source resistance of input FET, $R_{gs2} =$ gate-to-source resistance of output FET. $(K2)^2(\max)$ is identical to that of a single FET's maximum gain (stable). S-parameter data at 5.5 GHz evaluates $G\max$ of 12.9 dB. The overall power gain of the amplifier is $(K1K2K3)^2$, which is about 10 dB at the high frequency end, and which can be equalized across the entire band.

Fig. 3 illustrates the 0.47-in by 0.63-in distributed amplifier layout and final schematic showing all circuit elements. The amplifier is constructed on Rogers 5880 Duroid. The capacitors ($C1$–$C8$) provide either low impedance dc blocking or RF bypass. Inductor $L8$ provides a bias inject to both transistors, which are connected in series with respect to dc, conserving current (power). Voltage



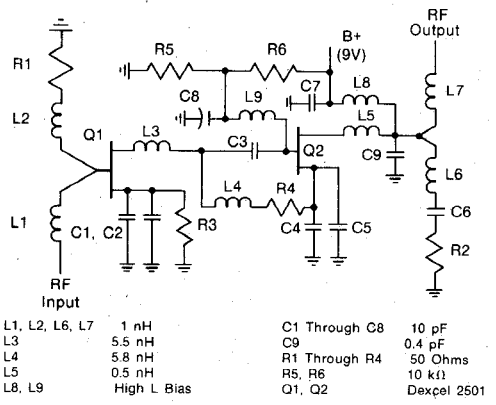


Fig. 3. Distributed amplifier layout and schematic.

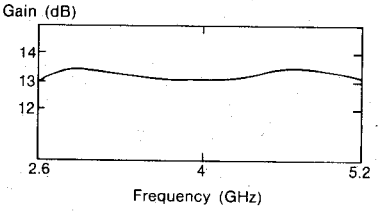
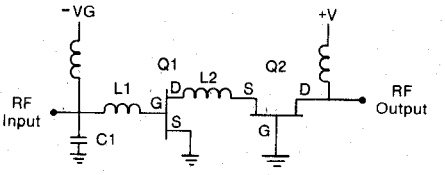


Fig. 4. Distributed amplifier gain response.

drops across $R3$ and $R4$, in conjunction with the dc voltage supplied through inductor $L9$, provides gate bias for both FET's. The additional $L5$–$C9$ circuit elements on the output of $Q2$ FET were required for minimum deviation of the gain across the frequency band.

Computer optimization yielded a flat gain of 10 ± 0.25 dB and a maximum VSWR of 1.4:1 over the range 2.6 to 5.2 GHz, with 55 ± 5 dB of reverse isolation. The measured gain of the amplifier (Fig. 4) was 13.25 ± 0.25 dB, somewhat higher than the computer-generated values, with a



Frequency	IF Band (2.6 - 5.2 GHz)	RF Band X-Band
Q1, Q2	Dexcel 3615	HP 5001
L1 (nH)	1.67	0.4
L2 (nH)	2.9	0.81
C1 (pF)	0.04	0.4
Calc Gain (dB)	10.9 ± 0.4	8.9 ± 0.4
Meas Gain (dB)	11 ± 0.5	12 ± 0.6
Measured P_o (dBm) for 1 dB Gain Compression	23	13

Fig. 5. Cascode amplifier.

TABLE II
S–*C* BAND CASCODE AMPLIFIER GAIN VERSUS FREQUENCY FOR VARIOUS CIRCUIT CONFIGURATIONS

	Gain (dB)						
Frequency (GHz)	1	2	3	4	5	6	7
2.5	7.76	1.61	8.08	8.61	9.21	10.17	10.50
3.0	7.27	1.61	7.64	8.36	9.16	10.36	10.80
3.5	6.83	1.62	7.24	8.17	9.21	10.53	11.05
4.0	6.44	1.65	6.86	8.04	9.30	10.65	11.22
4.5	6.10	1.73	6.61	8.06	9.51	10.70	11.27
5.0	5.76	1.85	6.33	8.11	9.79	10.55	11.07
5.5	5.40	1.98	6.09	8.27	10.00	10.33	10.74
C1(pF)	0	0	0	0	0	0.05	0.04
L1(nH)	0	0	0	0	0	1.5	1.67
L2(nH)	0	0	0	1.86	4	2.3	2.9
Note	A	B	C	C	C	C	C

Note A - Input Common Source FET Q1 Only
Note B - Output Common Gate FET Q2 Only
Note C - Cascode Configuration

maximum VSWR of 1.6:1 and an output 1-dB gain compression power of 10 dBm.

D. Cascode Amplifier

Matching of medium and high power amplifiers over wide bandwidths generally requires [2] multisection input and output matching networks or a combination of these networks with lossy feedback [3]. A novel cascade circuit has been developed for this module, both at the IF and RF bands, which achieves high gain and improved bandwidth capabilities with a simple interconnection network between the FET's as depicted in Fig. 5. The drain of the input common-source FET is connected through inductor $L2$ to the source of the output common-gate FET.

The inductor provides natural broad-band flat internal matching. The input shunt-C, series-L network provides additional gain. The net effect is a flat gain versus frequency with a 1-dB output power compression point that is fairly constant over the operating frequency range. The unit is very compact, since inductance values required for matching are low and readily obtained with bond wires. The amplifiers exhibit high input and output VSWR's and are used in a balanced arrangement using 3-dB Lange couplers.

Table II depicts the computed gain across the 2.5 to 5.5-GHz band using the Dexcel 3615 medium power chips with various combinations of circuit elements. Column 1 and column 2 illustrate the respective untuned gain of the

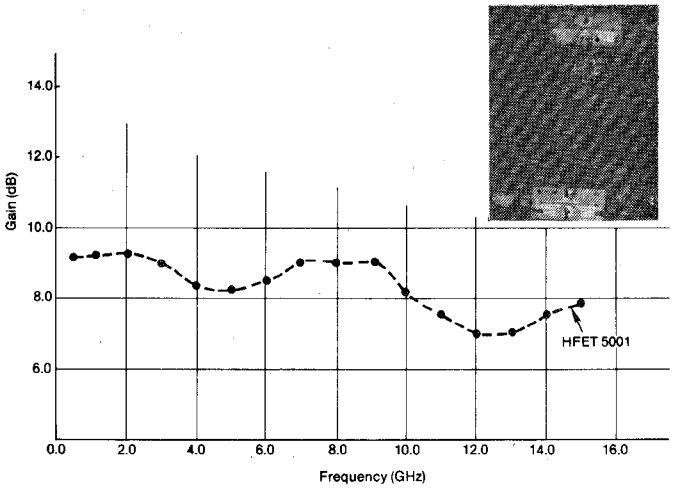


Fig. 6. Multioctave cascode amplifier performance.

first common source FET and second common gate FET individually, while column 3 illustrates the gain of the two stages cascaded with no additional matching elements. The overall gain is slightly less than the sum of the individual gain when cascaded since the input impedance of the second-stage common gate FET across the frequency range is 33-Ω real, not much different from 50 Ω. As the value interstage inductance ($L2$) is raised, the overall gain of the amplifier is increased. With $L2 = 1.86$ nH, a minimum gain variation over the band exists with an overall gain of 8.33 ± 0.29 dB as shown in column 4. As the inductance is increased to 4 nH, the gain at the high frequency is maximized to 10 dB with a low-frequency gain value of 9.21 dB as shown in column 5. This condition approximates interstage matching at the high frequency. Further increase of inductance reduces the gain at the high frequency. Adding the input shunt capacitance and series inductance ($C1-L1$) elements to the input of the input common source transistor raises and flattens the gain to a value of 10.4 ± 0.25 dB across the band as shown in column 6. A slight redistribution of circuit elements as shown in column 7 results in a higher gain of 10.9 ± 0.4 dB with a slight increase of gain variation across the band. The measured gain of the $S-C$ band cascode amplifier was 11 ± 0.5 dB, very close to the estimated value.

HP 5001 medium power chips were used for the X-band cascode amplifier. The equivalent circuit for the input impedance of the common gate output stage, accurate to 10 GHz, is a 35-Ω resistor in parallel with a 0.2-pF capacitor. Above 10 GHz, the resistor's value increases with frequency and reaches 50 Ω at 15 GHz. The equivalent circuit of the output impedance of the common source input stage, fairly accurate to 15 GHz, is a 220-Ω resistor in parallel with a 0.125-pF capacitor. The inductance between the stages, the value of which is selected to minimize the interstage mismatch at the high frequency end of the band, results in a calculated gain of 6.6 to 4.9 dB, decreasing in value across the band. With the added $C1-L1$ input circuit selected for flat gain, the overall gain was computer-optimized to 8.9 ± 0.4 dB. Optimization at higher gains results in a larger gain variation across the band. The actual measured gain when adjusted for high gain with minimum gain variation was 12 ± 0.6 dB over a 30-percent RF bandwidth.

An X-band unbalanced unit was retuned to demonstrate the wide-band capability of the cascode amplifier, the result being a gain of 8 ± 1 dB from 250 MHz to 15 GHz as shown in Fig. 6.

E. High-Level Mixer

A planar doubly balanced high-level mixer has been developed using microstrip, coplanar line, and slotline. The mixer uses a combination of techniques reported by de Ronde [4], Aikawa [5], and Dickens [6], [7]. Fig. 7 illustrates the converter planar layout, and Fig. 8 shows the top and bottom views of the converter mounted on a test fixture. The topside circuit consists entirely of microstrip circuitry, including the RF and IF ports, while the bottom has the slotline and coplanar line with the diode quad embedment circuits and LO port. The center conductor of the LO coaxial port on the bottom side is connected through the dielectric to the topside microstrip LO port location.

The RF signal is introduced to the two arms of the top microstrip circuit out of phase through the microstrip-to-slotline and slotline-to-microstrip transitions. The LO signal is introduced to the two arms of the microstrip circuit in phase. Due to the in-phase, out-of-phase relationships between RF and LO, a high degree of isolation exists between the RF and LO ports.

The RF and LO signals are next transferred to the figure-eight coplanar circuit on the bottom side through the two microstrip line to coplanar transitions. These signals traverse to the diode quad, which is located at the center of the figure-eight circuit as shown in Figs. 7 and 9. The LO turns on opposite diodes alternately (1 and 3, or 2 and 4) depending on the polarity of the signal. This alternates the polarity of RF signal across the slot from node a to node b at the LO rate. The RF modulated through a reversing switch at the LO rate generates the IF (doubly balanced mixer). The polarity of the IF is correct for transition back to the topside slotline-to-microstrip transition. An alternate method of considering the mixer operation is to consider the polarity of the IF signal generated in each diode and summing the resultant IF output as shown in Fig. 7. A high degree of isolation exists between the RF and LO ports to the IF port since these signals do not couple to the IF port through the transition.

The unitized eight-diode high-barrier silicon beam-lead ring quad was manufactured by Alpha Industries (DMJ 4759). Two high-barrier Schottky diodes with a combined voltage drop of 1.1 V for 1-mA forward current are located on each of the four sides of the rectangular ring quad. The quad measures 0.025 by 0.025 in, excluding the bonding tabs, and it terminates the four 0.016-in wide slots with minimal parasitics as shown in Fig. 9. The converter exhibited a third-order intercept point of +28 dBm (input), conversion loss of 7.5 ± 0.5 dB, maximum spurious response of −45 dBc for a signal level of +6 dBm, 1-dB gain compression at +13-dBm input power, maximum VSWR of 1.5 : 1, and minimum isolation of 25 dB between

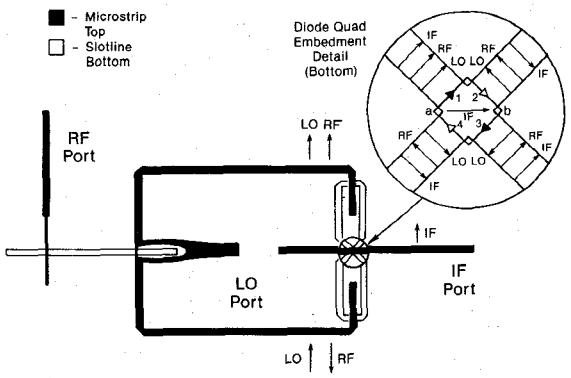


Fig. 7. High-level frequency converter layout.

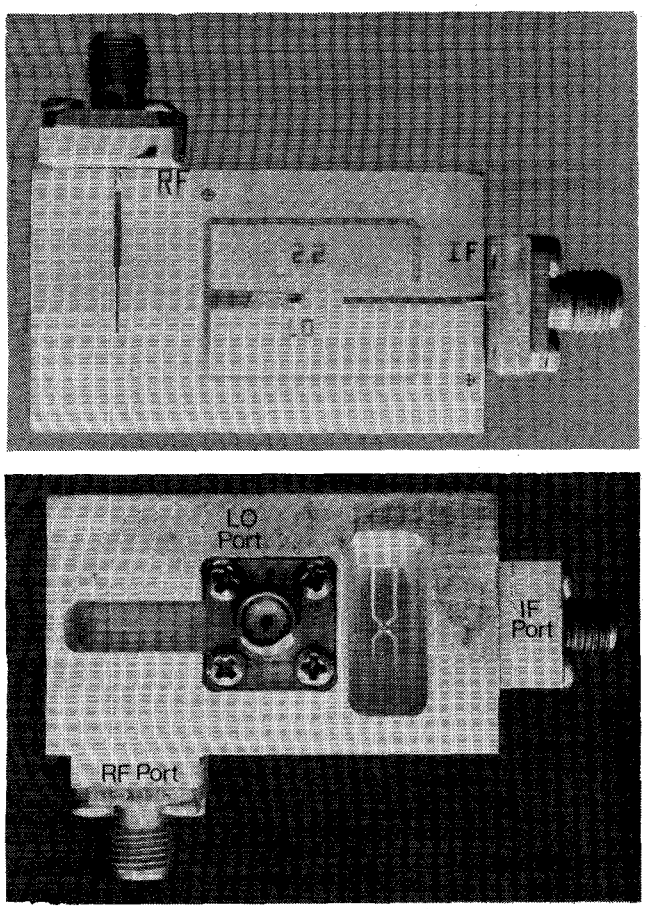


Fig. 8. Mixer test fixture.

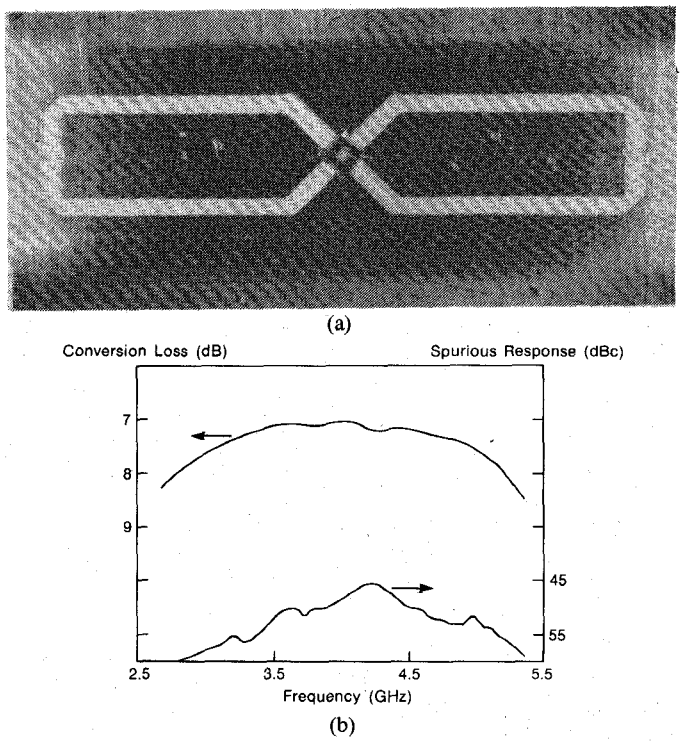


Fig. 9. High-level frequency converter (a) diode quad embedment detail and (b) performance.

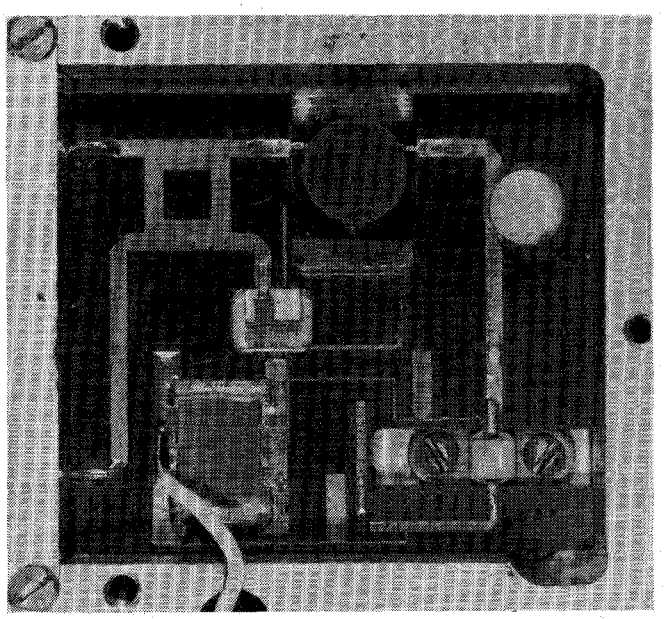


Fig. 10. Dielectric resonator FET oscillator.

any port across the 2.6 to 5.2-GHz IF band (see Fig. 9). The mixer used 23-dBm LO power at *Ku*-band with *X*-band RF frequency. Identical mixers were used for downconversion and upconversion and were constructed on Epsilam 10. The high third-order intercept point is a result of the use of the eight high-barrier diode ring quad driven with high LO power as opposed to a four low-barrier diode quad and the diode quad embedment circuitry.

F. Dielectric Resonator FET Oscillator (DRO)

Fig. 10 illustrates the *Ku*-band FET DRO on Duroid microstrip. A flange-mounted packaged MSC 88004 power FET provided 0.5 W of output power (14-percent efficiency) when stabilized. An open-circuited stub on the gate at optimum length provides peak negative resistance when the transistor's output drain terminal is biased negative with respect to ground. A puck of Transtec D-38 is strategically located on the output circuit to lock the frequency to within ± 3 MHz from $-55°C$ to $95°C$. A microstrip ferrite isolator cascaded by a branch-line hybrid coupler provides two 23-dBm outputs to drive each mixer.

III. Conclusions

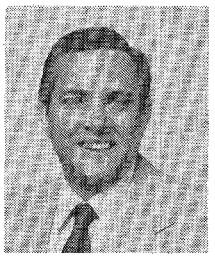
Novel broad-band circuits coupled with advanced large-scale-integration techniques have led to the development of a high-performance, compact microwave module.

ACKNOWLEDGMENT

The authors wish to thank J. Gipprich, S. Payer, and G. Lutor for their participation in this development.

REFERENCES

[1] J. A. Archer, F. A. Petz, and H. P. Weldlich, "GaAs FET distributed amplifier," *Electron. Lett.*, vol. 17, p. 433, June 1981.
[2] R. L. Camisa, J. B. Klatskin, and A. Mikelsons, "Broad-band lumped-element GaAs FET power amplifiers," in *1981 MTT-S Int. Microwave Symp.*, June 1981, pp. 126–128.
[3] K. B. Niclas, "Compact multi-stage single-ended amplifiers for $S-C$ band operation," in *1981 MTT-S Int. Microwave Symp.*, June 1981, pp. 132–134.
[4] F. C. de Ronde, "A new class of microstrip directional couplers," in *G-MTT 1970 Int. Microwave Symp.*, May 1970, pp. 184–189.
[5] Masayoshi Aikawa and Hiroyo Ogawa, "2-Gb, double-balanced PSK modulator using coplanar waveguides," in *1979 Int. Solid-State Circuits Conf.*, Feb. 1979, pp. 172–173.
[6] L. E. Dickens and D. W. Maki, "A new phased-type image enhanced mixer," in *1975 MTT-S Int. Microwave Symp. Dig.*, May 1975, pp. 149–151.
[7] L. E. Dickens and D. W. Maki, "An integrated-circuit balanced mixer, image and sum enhanced," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, Mar. 1975.



Edward C. Niehenke (M'61–SM'81) was born in Abington, PA, on August 5, 1937. He received the B.S. (1961) and M.S. (1965) degrees in electrical engineering from Drexel University, Philadelphia, PA. In 1970 he completed additional course work in electrophysics at the University of Maryland, College Park, MD.

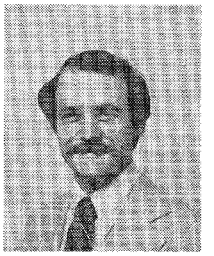
From 1961 to 1963, he was employed by Martin Marietta, Baltimore, MD, where he was engaged in the investigation of solid-state device behavior at cryogenic temperatures and low-loss cryogenic superconducting delay lines. Since 1963, he has been employed by Westinghouse Electric Corp., Systems Development Division, Baltimore, responsible for the development of low-noise broad-band parametric amplifiers, FET amplifiers, limiters, voltage controlled oscillators, FET dielectric resonator oscillators, mixers, and miniature microwave integrated circuits. His present duties as Advisory Engineer for Microwave Operations include consultation and development of microwave circuitry for radar and ECM systems with emphasis on low-noise techniques. He holds four patents in the microwave area and has authored numerous papers on microwave circuits.

Mr. Niehenke is a registered Professional Engineer in the state of Maryland. He has held various positions including Chairman of the Baltimore AP/MTT chapter. He is a member of MTT-S ADCOM serving as Membership Chairman and is a Director of Programs for the Baltimore IEEE Section. He is a member of MTT-S Microwave and Millimeter Wave Integrated Circuits Technical Committee as well as MTT-S Waveguide Standards Committee and is Chairman of the 1986 MTT-S International Microwave Symposium to be held in Baltimore, MD.

Rick D. Hess (M'79) was born in Kokomo, IN, on June 14, 1953. He received the B.S. degree in electrical engineering from Purdue University, Lafayette, IN, in 1975, and the M.S. degree in electrical engineering from Johns Hopkins University, Baltimore, MD, in 1982.

He was employed by Westinghouse Electric Corp., Baltimore, MD, from 1975 to 1981. He is presently President of Stable Energy Sources, Lancaster, PA. He has been involved in the development of digital microwave frequency translators at X-band and Ku-band. He has developed high-power and low-noise amplifiers at X-band, as well as low-noise voltage-controlled oscillators at L-and X-bands. He has also designed high density microwave integrated circuitry.

Mr. Hess is a member of Eta Kappa Nu and the Microwave Theory and Techniques Society.



Jed S. Rosen received the B.S. degree in electrical engineering from Columbia University, New York, in 1976.

He joined Westinghouse Electric Corp. in 1976 and is currently a Senior Engineer in the Systems Development Division, Microwave Operations. He has been engaged in the design of broad-band isolators, mixers, and low-noise amplifiers, and in computer aided design and testing. He is presently pursuing an M.D. at the University of Maryland School of Medicine.

Mr. Rosen is a member of Eta Kappa Nu and Tau Beta Pi.

Lawrence E. Dickens (A'56–M'59–SM'69–F'77) was born in North Kingstown, RI, on December 8, 1932. He received the B.S. and M.S. degrees in engineering and the D.Eng. degree in 1960, 1962, and 1964, respectively, from Johns Hopkins University, Baltimore, MD.

After his military service (1950–1953), he joined Bendix Radio, Field Engineering, Baltimore, MD. In 1956 he transferred to the Department of Research and Development (Radar) at Bendix Radio where he worked on vacuum tube, transistor, tunnel diode, and parametric (reactance) amplifiers. From 1960 to 1965 he worked at the Carlyle Barton Laboratory of Johns Hopkins University where he was engaged in the investigations of circuits and materials with the general objective of improving microwave and millimeter-wave receiving systems. From 1965 to 1969 he was on the staff of the Advanced Technology Corp., Timonium, MD, where he was engaged in the development of semiconductor components and the RF and millimeter-wave circuits for their utilization. In 1969 he joined the staff at Westinghouse Electric Corp. Systems Development Division, Advanced Technology Laboratories, as an Advisory Engineer where he has been engaged in the development of microwave solid-state devices, RF, microwave, and millimeter-wave circuitry, microwave integrated circuits, and more recently gallium arsenide microwave monolithic circuits.

Joseph A. Faulkner, Jr. (M'81) received the B.S.E.E. from Duke University, Durham, NC, in 1978.

Upon graduation he came to work in the Microwave Operations group under the Systems Development Division at the Westinghouse Electric Corp. in Baltimore, MD. He is currently a Senior Engineer at Westinghouse and has worked on the design and development of low-noise amplifiers, power amplifiers, voltage-controlled oscillators, switches, attenuators, couplers, and other microwave hardware for radar applications.

Mr. Faulkner is a member of Tau Beta Pi and Phi Beta Kappa. He is presently the Secretary/Treasurer for the Baltimore AP/MTT Chapter of IEEE.